Application Report
SLAA666A–March 2015–Revised January 2020

Differences Between MSP430F67xx and MSP430F67xxA Devices

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ABSTRACT

This application report describes the enhancements of the MSP430F67xxA devices from the non-A MSP430F67xx devices. In the course of this application report, the MSP430F67xx errata that are fixed in the MSP430F67xxA and the additional features added to the MSP430F67xxA devices are discussed. In addition, metrology results are compared to further show that the changes implemented in the MSP430F67xxA devices do not affect the metrology performance.

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1 Introduction

The MSP430F67xxA devices are the latest e-meter SoCs from Texas Instruments for 1-phase and 3-phase meters. These devices offer enhancements from the previous non-A MSP430F67xx e-meter SoCs while still maintaining all of the features of the non-A chips so that a non-A device can be replaced with the corresponding A version of that chip. As an example, this would allow a MSP430F6736-based design to be upgraded by swapping its MSP430F6736 with a MSP430F6736A. This can be done for all of the F67xxA chips, which are all mentioned below:

- MSP430F672xA and MSP430F673xA single-phase metering SoCs
- MSP430F676x1A low-cost poly-phase metering SoCs
- MSP430F677xA, MSP430F676xA, MSP430F674xA, MSP430F677x1A, MSP430F676x1A, and MSP430F674x1A high-accuracy poly-phase metering SoCs

Note that the "A" in the MSP430F67xxA devices is listed on a chip as a part of the part number and is independent of the letter listed as the silicon revision number. For example, a non-A device may be labeled on the chip as being "Rev A" but is still considered a non-A device. Similarly, a MSP430F67xxA device may say "Rev B" but is still a MSP430F67xxA chip. Care must be taken not to confuse the revision letter on the chip with being a part of the chip part number.

Also, when comparing the MSP430F67xx non-A devices to the MSP430F67xxA devices, the following changes were made onto the MSP430F67xxA:

- Errata AUXPMM1 and RTC8 have been fixed.
- An RTCLOCK feature has been added to the RTC.
- A modification was made to better address ESD robustness.

2 Fixed Errata

One erratum in the non-A MSP430F67xx devices was the AUXPMM1 errata that is listed in the device erratasheets. This erratum covers the AUX module, which is a module that allows switching the supply that powers the chip from DVCC/AVCC to AUXVCC1 or AUXVCC2 if DVCC/AVCC falls below a certain voltage threshold. After DVCC/AVCC rises above the associated threshold, the chip should automatically switch back to being powered by DVCC/AVCC. However, in this erratum, there could be a case where the AUX module would not switch back to DVCC when it is running from AUXVCC1 or AUXVCC2. In particular, when the system is running with the AUXVCC1/AUXVCC2 supply after DVCC/AVCC is lost, and if the AUXVCC1 voltage goes lower than the SVSH setting for POR but above the BORH level, the system cannot switch back to DVCC after DVCC ramps back up again. In a typical application, DVCC/AVCC is powered from mains through a power supply, while AUXVCC1 or AUXVCC2 are connected to batteries. As a result of this configuration and this erratum, the chip would continue to be powered from the battery despite Mains being present. This would eventually lead to the battery being depleted. In the MSP430F67xxA devices, this erratum has been fixed, which prevents this sequence of events from happening.

Another erratum fixed in the MSP430F67xxA devices was the RTC8 erratum mentioned in device erratasheets. This particular erratum is most pertinent to the high-accuracy poly-phase metering SoCs, because they have the RTCCAP functionality present. For this RTCCAP feature, whenever there is an event (a rising or falling edge) detected on any of the RTCCAP pins, the RTC time when this occurs is logged. In a typical application, the RTCCAP pins could be connected to a meter case so that whenever someone tries to open the case, a switch would trip and send a rising or falling edge signal to the RTCCAP pin. From there, the time of this case tamper event could be logged.

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In the F67xx devices, the backup subsystem that includes the RTC is powered independently by AUXVCC3 (instead of by DVCC/AVCC, AUXVCC1, or AUXVCC2). Because the rest of the chip does not need to be powered, this reduces the current draw when only the RTC needs to be functional. However, due to the RTC8 erratum, the tamper detection function triggered by the RTCCAP0 and RTCCAP1 pins cannot get a correct time stamp value when DVCC and AUXVCC1 are off. To ensure that the correct time stamp is obtained, DVCC and AUXVCC1 should not be off. As a result, the current draw is increased when this feature is necessary. For the MSP430F67xxA devices, this erratum is fixed so that the correct time stamp can be captured with only voltage at AUXVCC3 present, thereby preventing the increase in current from having to power the rest of the chip via DVCC/AVCC, AUXVCC1, or AUXVCC2.

3 Addition of RTCLOCK Feature

In the MSP430F67xxA devices, a RTCLOCK feature has been added to reduce the amount of reconfigurations that are necessary after a reset. The RTCLOCK feature is enabled by setting the RTCLOCK bit in the RTC's RTCCTL3 register. By setting this bit, it locks all LPM3.5 retention logic from write and reset operations as long as a power cycle on AUXVCC3 does not occur. This locking mechanism is accomplished by having LPM3.5 retention logic either locked or powered from AUXVCC3 instead of VDSYS. One thing to note is that if RTCLOCK is set, the configuration of the bits locked by RTCLOCK may be held but not the bits themselves (i.e. the value of affected bits in the debugger may not reflect the actual configuration when the RTCLOCK feature is enabled). RTCLOCK may need to even be reset before reinitialization of some RTC registers such as the RTC time and date registers.

One benefit of this RTCLOCK feature is that it prevents having to clear the RTCHOLD bit after a POR reset. This prevents the RTC from being stopped when exposed to a pulse on VCC that is long enough to set the RTCHOLD bit but not long enough to allow software to clear RTCHOLD. For instance, if a battery is connected to AUXVCC3 only, AUXVCC1 and AUXVCC2 are not used as alternative power supplies, and power is lost at DVCC/AVCC, the RTC would still continue to count. However, when power is restored, a POR event would occur and the RTCHOLD bit would automatically be set causing the RTC to be turned OFF. This RTCHOLD bit should be cleared as soon as possible so that the RTC can continue counting from where it was before RTCHOLD was set. As a result of having to turn off RTCHOLD, the RTC time is off by the time difference between when the RTCHOLD bit was set and when it was cleared in software. Additionally, there could be a case where power at DVCC/AVCC is restored long enough so that RTCHOLD is set but not long enough for the software to clear this bit, thereby causing the RTC to stop. However, with the RTCLOCK feature there is no need to clear the RTCHOLD bit, thereby preventing this from happening.

When using the RTCLOCK feature, the RTCLOCK bit should be set after RTCHOLD is cleared to allow the RTC to start counting. For a code example that shows how to use the RTCLOCK bit, refer to the TI Design Battery Management and Auxiliary Power Supply Options for E-Meters (TIDM-AUX-MODULE).

4 ESD Robustness

To address ESD robustness, certain logic was moved from one location in the chip to another. This change was not done on any modules that are critical for metrology. Additionally, ESD tests with respect to e-meters are system-level tests. Therefore, bolstering the chip's ESD performance may not compensate for any ESD issues that arise due to design weaknesses.

TI recommends following ESD guidelines and performing proper ESD testing when creating a new design or when migrating between devices. Recommendations include following PCB layout recommendations, using ESD protection devices, enabling NMI interrupts to detect or prevent unexpected resets, and enabling the oscillator fault interrupt to detect oscillator disturbances. For more guidelines and recommendations on how to create robust system-level designs, see *MSP430 System-Level ESD Considerations*.

To test the comparative ESD robustness of the MSP430F67xxA, an IEC 61000-4-2 test was performed on one EVM430-F6779 (see Figure 1 for EVM picture) that had the MSP430F67791A as the metering SoC and another EVM430-F6779 that had the non-A MSP430F67791 as the metering SoC. For the EVM430-F6779, some ESD tradeoffs were made to support fully showcasing the features of the silicon and ease of use for evaluation purposes. However, the EVM can still be used as a gauge to show the improvements of the MSP430F67xxA devices.

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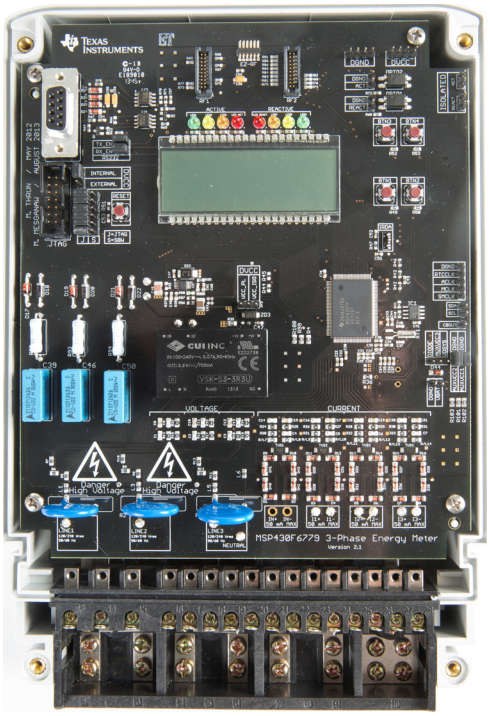

Figure 1. EVM430-F6779

For applying the ESD test on the two test EVMs, both positive and negative polarity discharges were applied on both test boards at the same location. In the tests, recoverable failures (for example, a reset), lock-ups, and latch-ups were logged as failures. Because the only items that differed between the two tested boards was whether a MSP430F67791A or MSP430F67791 was installed, this test shows the additional robustness due to upgrading to the A version of the MSP430F67xx chips. Table 1 shows the results of these tests:

Table 1. IEC 61000-4-2 Test Results for the MSP430F67791 and MSP430F67791A

Test Voltage (kV)	F67791 Results (+ polarity / – polarity)	F67791A Results (+ polarity / – polarity)
1	Pass / Pass	Pass / Pass
2	Pass / Pass	Pass / Pass
4	Pass / Pass	Pass / Pass
6	Pass / Pass	Pass / Pass
8	Pass / Pass	Pass / Pass
10	Fail / Pass	Pass / Pass
12	Fail / Fail	Pass / Pass
14		Pass / Pass
16		Pass / Pass
18		Pass / Pass
20		Pass / Pass

As shown in the table, by upgrading the MSP430F67791 chips in the EVM430-F6779 with the MSP430F67791A, the ESD robustness improved at the test point by at least 8-10 kV. In addition, the F67791A results would pass even level 4 of IEC 61000-4-2. For more details on these MSP430F67791(A) ESD tests, refer to the TI Design Three-Phase Metrology with Enhanced ESD Protection and Tamper Detection (TIDM-3PHMTR-TAMP-ESD).

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In addition to performing ESD tests on the EVM430-F6779, a similar test was performed with one EVM430-F6736 (see Figure 2 for an EVM picture) that had the MSP430F6736A and another one that had the MSP430F6736. For testing the EVM430-F6736, the ESD strike was applied at four locations: near the top, bottom, left, and right of the EVMs. Table 2 through Table 5 show the results of these tests.

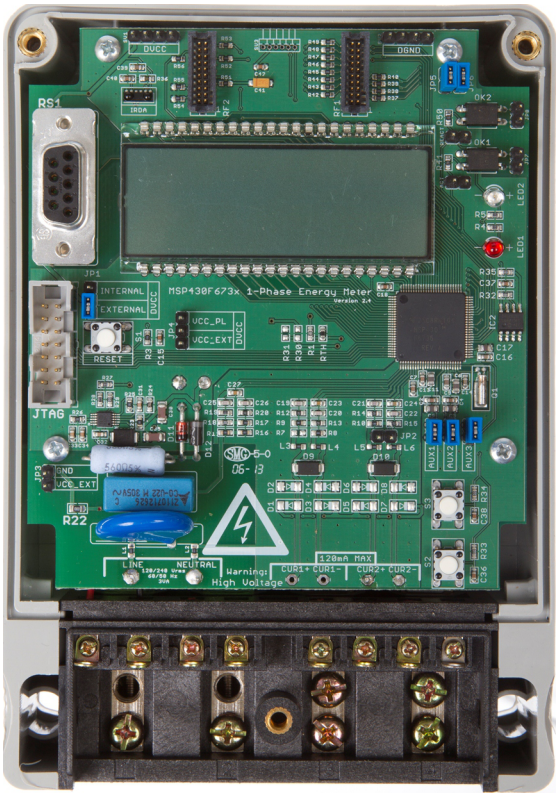

Figure 2. EVM430-F6736

Table 2. IEC 61000-4-2 Test Results for the MSP430F6736 and MSP430F6736A, ESD Gun Applied Near the Left of the EVM

Test Voltage (kV)	F6736 Results (+ polarity / – polarity)	F6736A Results (+ polarity / – polarity)
2	Pass / Pass	Pass / Pass
4	Pass / Pass	Pass / Pass
6	Pass / Pass	Pass / Pass
8	Pass / Pass	Pass / Pass
10	Pass / Pass	Pass / Pass
12	Pass / Pass	Pass / Pass
14	Pass / Pass	Pass / Pass
16	Pass / Pass	Pass / Pass
18	Pass / Pass	Pass / Pass
20	Pass / Pass	Pass / Pass

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Table 3. IEC 61000-4-2 Test Results for the MSP430F6736 and MSP430F6736A, ESD Gun Applied Near the Right of the EVM

Test Voltage (kV)	F6736 Results (+ polarity / – polarity)	F6736A Results (+ polarity / – polarity)
2	Pass / Pass	Pass / Pass
4	Pass / Pass	Pass / Pass
6	Pass / Pass	Pass / Pass
8	Pass / Pass	Pass / Pass
10	Pass / Pass	Pass / Pass
12	Pass / Pass	Pass / Pass
14	Pass / Pass	Pass / Pass
16	Fail (Anomaly) / Pass	Pass / Pass
18	Pass / Pass	Pass / Pass
20	Fail / Pass	Pass / Pass

Table 4. IEC 61000-4-2 Test Results for the MSP430F6736 and MSP430F6736A, ESD Gun Applied Near the Bottom of the EVM

Test Voltage (kV)	F6736 Results (+ polarity / – polarity)	F6736A Results (+ polarity / – polarity)
2	Pass / Pass	Pass / Pass
4	Pass / Pass	Pass / Pass
6	Pass / Pass	Pass / Pass
8	Pass / Pass	Pass / Pass
10	Pass / Pass	Pass / Pass
12	Pass / Pass	Pass / Pass
14	Pass / Pass	Pass / Pass
16	Pass / Pass	Pass / Pass
18	Pass / Fail - Pass	Pass / Pass
20	Pass / Fail	Pass / Pass

Table 5. IEC 61000-4-2 Test Results for the MSP430F6736 and MSP430F6736A, ESD Gun Applied Near the Top of the EVM

Test Voltage (kV)	F6736 Results (+ polarity / – polarity)	F6736A Results (+ polarity / – polarity)
2	Pass / Pass	Pass / Pass
4	Pass / Pass	Pass / Pass
6	Pass / Pass	Pass / Pass
8	Pass / Pass	Pass / Pass
10	Fail / Pass	Pass / Pass
12	Fail / Fail	Pass / Pass
14	/ Fail	Pass / Pass
16		Pass / Fail (Anomaly) - Pass
18		Fail / Fail
20		Fail /

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These tables show that replacing a MSP430F6736 with a MSP430F6736A could improve a design's ESD robustness. For more details on these MSP430F6736(A) ESD tests, refer to the TI Design One-Phase Metrology with Enhanced ESD Protection (TIDM-1PHMTR-ESD).

5 Migration From the Non-A MSP430F67xx Devices to the MSP430F67xxA Devices

To migrate from a non-A MSP430F67xx device to its corresponding MSP430F67xxA device, minimal changes are necessary. A MSP430F67xx device and its corresponding MSP430F67xxA device are pin-to-pin compatible, so a non-A chip can physically be replaced with an A version. Additionally, the software on a MSP430F67xx device should also run on a MSP430F67xxA device as long as the software is updated to correspond to the proper header files and device name in the IDE project settings.

6 Metrology Results

With the changes made onto the MSP430F67xxA, the metrology performance should still be comparable to the non-A MSP430F67xx devices. To show this, an EVM430-F6779 poly-phase EVM is tested with both a MSP430F67791 and a MSP430F67791A. For the tests, the software attached to the application report *Implementation of a Three-Phase Electronic Watt-Hour Meter Using MSP430F677x(A)* (SLAA577) is used to test the MSP430F67791. The same software was then modified to use the MSP430F67791A to test the metrology performance of the MSP430F67791A. The software used to test the MSP430F67791A is available with the TI Design TIDM-3PHMTR-TAMP-ESD.

Similarly, an EVM430-F6736 single-phase EVM is tested with both a MSP430F6736 and a MSP430F6736A. The MSP430F6736 was tested with the code that is available with the application report *Implementation of a Single-Phase Electronic Watt-Hour Meter Using MSP430F6736(A)* (SLAA517). This same code was then updated to correspond to the MSP430F6736 for performing metrology testing. This MSP430F6736A-based software is available with the TI Design TIDM-1PHMTR-ESD.

Table 6, Figure 3, and Figure 4 show the metrology results for the MSP430F67791 and MSP430F67791A. Table 7, Figure 5, and Figure 6 show the metrology results for the MSP430F6736 and MSP430F6736A. In both sets of results, the A version of the chips do not differ significantly from the non-A versions of the chips.

Table 6. Active Energy % Error for MSP430F67791 and MSP430F67791A

Current (Amps)	MSP430F67791			MSP430F67791A		
	0°	60°	-60°	0°	60°	-60°
0.05	-0.043	-0.086	-0.076	-0.011	-0.024	-0.08
0.1	-0.053	-0.019	-0.068	-0.005	0.077	-0.079
0.25	-0.028	-0.03	-0.057	-0.018	0.005	-0.078
0.5	-0.014	-0.018	-0.04	-0.027	-0.009	-0.058
1	-0.01	-0.004	-0.022	-0.015	0	-0.04
2	-0.0206667	-0.00166667	-0.039	-0.029	0.00166667	-0.0543333
5	-0.018	-0.015	-0.0123333	-0.0216667	-0.0113333	-0.0296667
10	-0.00733333	-0.0233333	0.0143333	-0.0126667	-0.017	-0.00833333
20	-0.00833333	-0.042	0.028	-0.0106667	-0.0273333	0.00666667
30	-0.000333333	-0.0646667	0.062	-0.005	-0.043	0.0393333
40	-0.003	-0.091	0.078	-0.00233333	-0.0606667	0.0563333
50	-0.0143333	-0.122	0.0983333	-0.008	-0.101333	0.0786667
60	-0.009	-0.135	0.111333	-0.0106667	-0.113333	0.0863333
70	-0.0123333	-0.148667	0.12	-0.0113333	-0.120667	0.0963333
80	-0.011	-0.15	0.130333	-0.016	-0.131667	0.097
90	-0.014	-0.158667	0.126333	-0.018	-0.136	0.098
100	-0.027	-0.179333	0.119333	-0.0253333	-0.144333	0.0933333

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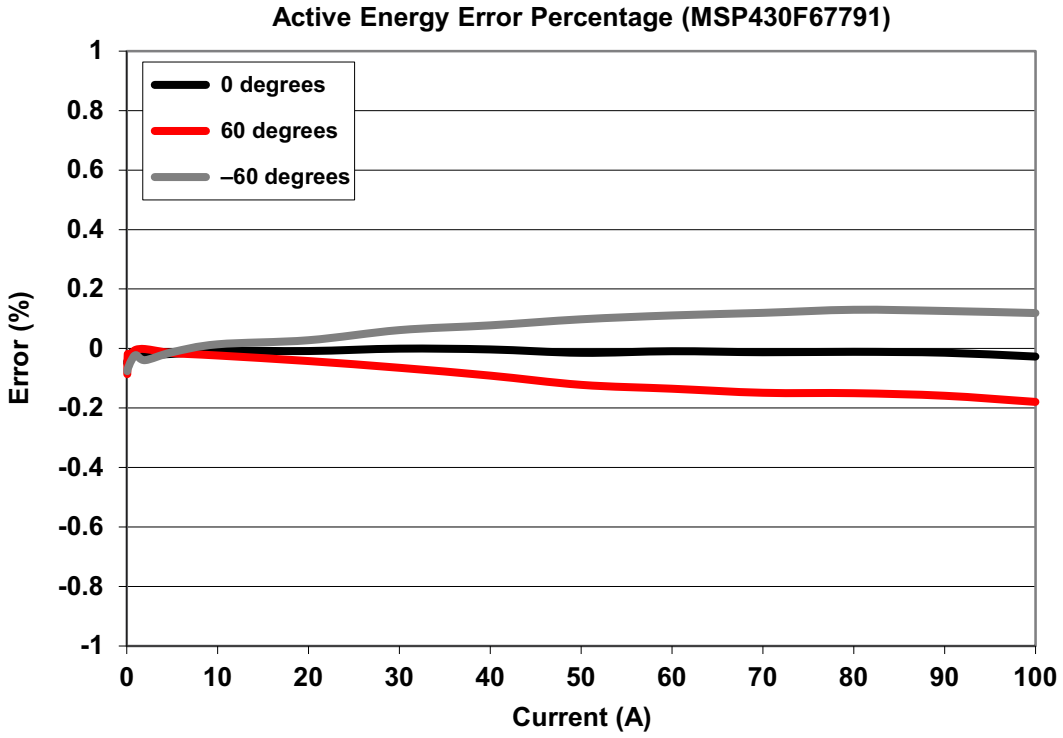

Figure 3. EVM430-F6779 Performance With MSP430F67791

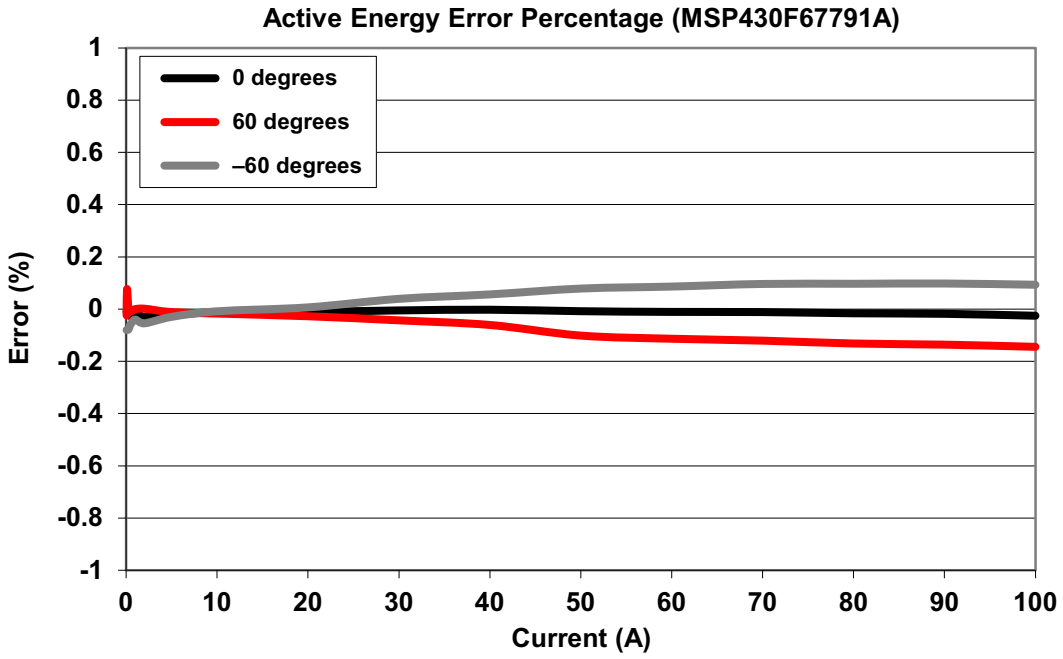

Figure 4. EVM430-F6779 Performance With MSP430F67791A

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Table 7. Active Energy % Error for MSP430F6736 and MSP430F6736A

Current (Amps)	MSP430F6736			MSP430F6736A		
	0°	60°	-60°	0°	60°	-60°
0.05	-0.045	0.058	-0.07	0.058	0.006	0.006
0.1	-0.019	0.083	-0.07	0.006	-0.019	0.006
0.25	-0.019	0.0575	-0.0575	0.006	0.032	-0.019
0.5	0.006	0.083	-0.045	-0.0023	0.0233	0.0063
1	0.0147	0.0663	-0.0617	0.0147	0.032	-0.0023
2	-0.007	0.058	-0.07	-0.007	0.0233	-0.019
5	0.0043	0.022	-0.019	0.008	0.011	0.017
10	-0.007	-0.024	0.003	0.014	-0.0007	0.03
20	-0.015	-0.0533	0.0493	0.006	-0.019	0.032
30	0.0003	-0.079	0.0747	0.015	-0.045	0.058
40	-0.0067	-0.096	0.07	0.019	-0.0493	0.0787
50	0.011	-0.106	0.1023	0.03	-0.055	0.119
60	0.0006	-0.099	0.1203	0.032	-0.0643	0.123
70	0.0167	-0.096	0.1187	0.0307	-0.067	0.1307
80	0.0263	-0.098	0.143	0.035	-0.064	0.1407
90	0.0367	-0.096	0.1563	0.043	-0.062	0.1467
100	0.0387	-0.0943	0.16	0.04	-0.06	0.155

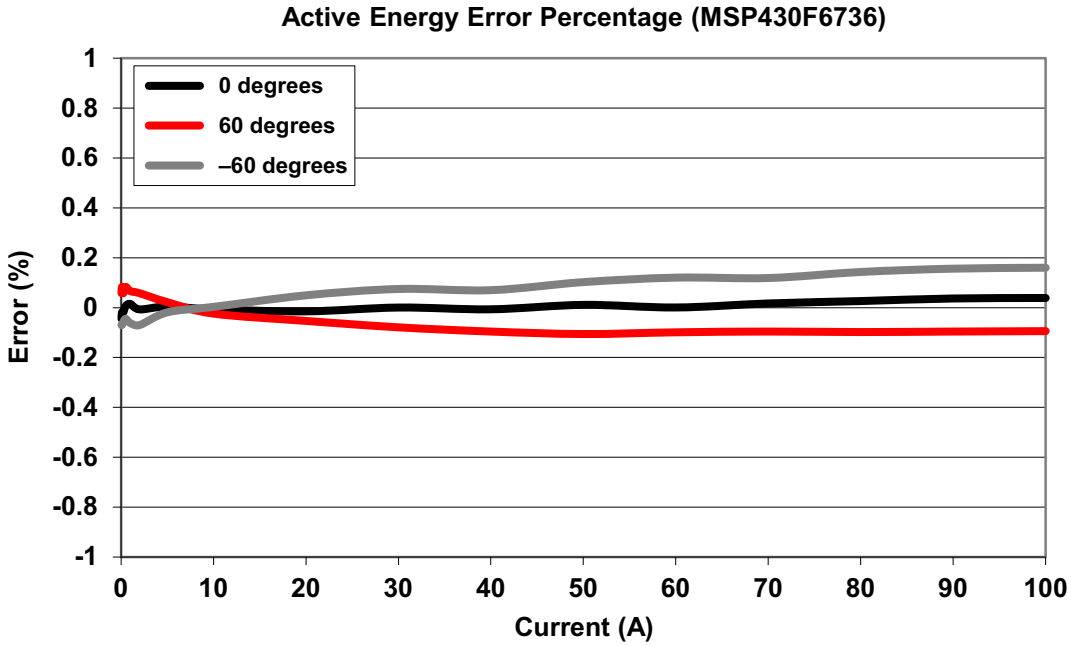

Figure 5. EVM430-F6736 Performance With MSP430F6736

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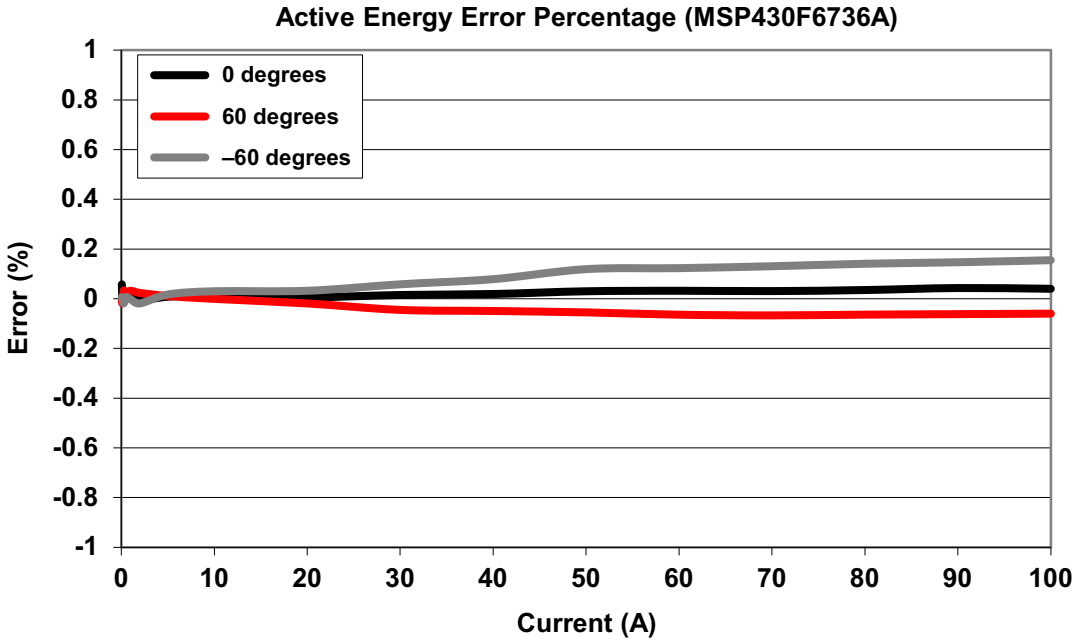

Figure 6. EVM430-F6736 Performance With MSP430F6736A

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Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from March 30, 2015 to January 13, 2020	Page
• Added the paragraph that begins "TI recommends following ESD guidelines and performing proper ESD testing..." in Section 4, *ESD Robustness*	3

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