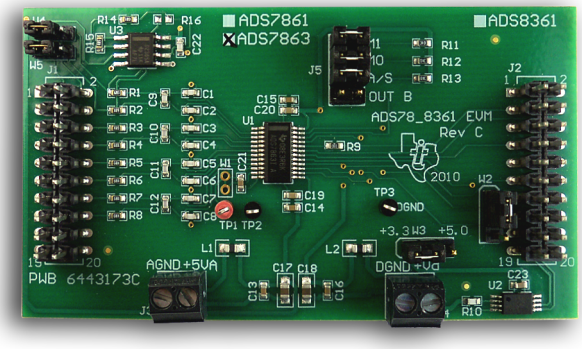
# ADS7861/8361/7863EVM




**ADS7861/8361/7863EVM**

This user's guide describes the characteristics, operation, and use of the ADS7861/8361/7863EVM. This evaluation model (EVM) is an evaluation board for the ADS7861, ADS7863, and ADS8361, a family of 12-/16-bit, dual, 500-kSPS, 2+2 channel, serial analog-to- digital converters (ADCs). The EVM allows evaluation of all aspects of the ADS7861/7863/8361 devices. Complete circuit descriptions, a schematic diagram, and a bill of materials are included in this document.

The following related documents are available for download through the Texas Instruments web site at http://www.ti.com.

**Related Documentation**

| Document | Literature Number |
|---|---|
| ADS7861 Product Data Sheet | SBAS110 |
| ADS7863 Product Data Sheet | SBAS383E |
| ADS8361 Product Data Sheet | SBAS230 |
| Op Amps for Everyone Design Guide | SLOD006B |

**Contents**



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# 1 EVM Overview

## 1.1 Features

**ADS7861/8361/7863EVM:**

- Full-featured evaluation board for the ADS7861, ADS8361, and ADS7863, dual, 500-kSPS, 12-bit/16-bit, serial output, 2+2 analog input, simultaneous sampling analog-to-digital converters
- Analog inputs can be configured as single-ended or differential
- Built-in reference
- High-speed serial interface

This manual covers the operation of the ADS7861EVM, ADS8361EVM, and the ADS7863EVM, collectively identified as *ADS7861/8361/7863EVM*. Throughout this document, the abbreviation *EVM* and the term *evaluation module* are synonymous with the ADS7861/8361/7863EVM. Unless otherwise indicated, all references to device operation apply to all three devices.

## 1.2 Introduction

The ADS7861 operates from 5 V for $AV_{DD}$ and $DV_{DD}$ while the ADS8361 operates from 2.7 V to 3.6 V for $AV_{DD}$ and $DV_{DD}$. The ADS7863 operates from 2.7 V to 5.5 V for $AV_{DD}$ and $DV_{DD}$. Each device is a high-speed, low-power, 12-bit or 16-bit A/D converter (ADC).

The four fully-differential analog inputs are divided into two pairs (A and B). Each ADC accepts an analog input voltage in the range of –VREF to +VREF (5 $V_{PP}$), centered on the internal 2.5-V reference. The device also accepts bipolar input ranges when a level shift circuit is used in the analog frontend circuitry. Refer to Section 12 of the Design Guide, *Op Amps for Everyone* (literature number SLOD006B) for information on various circuit applications.

# 2 Analog Interface

For maximum flexibility, the ADS7861/8361/7863EVM is designed for easy interfacing to multiple analog sources. Samtec part numbers SSW–110–22–F–D–VS–K and TSM–110–01–T–DV–P provide a convenient, 10-pin, dual row header/socket combination at J1. This header/socket provides access to the analog input pins of the ADC. Consult Samtec at http://www.samtec.com or call 1-800-SAMTEC-9 for a variety of mating connector options. Table 1 summarizes the pinouts for analog interfaces J1.

**Table 1. J1: Analog Interface Pinout**

| Pin Number | Signal | Description |
|---|---|---|
| J1.2 | B1+ | Noninverting input, channel B1 |
| J1.4 | B1– | Inverting input, channel B1 |
| J1.6 | B0+ | Noninverting input, channel B0 |
| J1.8 | B0– | Inverting input, channel B0 |
| J1.10 | A1+ | Noninverting input, channel A1 |
| J1.12 | A1– | Inverting input, channel A1 |
| J1.14 | A0+ | Noninverting input, channel A0 |
| J1.16 | A0– | Inverting input, channel A0 |
| J1.18 | Unused | Pins are unused and should be left open for use with future amplifier and sensor input modules. |
| J1.20 | REFIN | External reference source input (2.5 V nom, 2.525 V max) |
| J1.1 to J1.19 (odd) | AGND | Analog ground connections |


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# 3 Digital Interface

The ADS7861/8361/7863EVM is designed for easy interfacing to multiple control platforms. Samtec part numbers SSW–110–22–F–D–VS–K and TSM–110–01–T–DV–P provide a convenient, 10-pin dual row header/socket combination at J2. This header/socket provides access to the digital control and serial data pins of the ADS7861/8361. Consult Samtec at http://www.samtec.com or call 1-800-SAMTEC-9 for a variety of mating connector options. Table 2 describes the J2 serial interface pins.

**Table 2. J2: Serial Interface Pins**

| Pin Number | Signal | Description |
|---|---|---|
| J2.1 | $\overline{CS}$ | Chip select; active low signal, enables data transfer and device configuration |
| J2.3 | SCLK | Serial clock |
| J2.5 | SCLK(R) | Serial clock return for DSP host |
| J2.7 | FS | Frame sync |
| J2.9 | FS(R) | Frame sync return for DSP host |
| J2.11 | SDI | Serial data input |
| J2.13 | SDO | Serial data output |
| J2.15 | INT | Interrupt output; provides an interrupt source to the host processor |
| J2.17 | CSTART | Conversion start; provides an alternate method of conversion initialization |
| J2.19 | SPARE | |

## 3.1 Additional Control Options

Table 3 shows the pinout of header J5. This dual-row, four-position header provides additional control functionality to the ADS7861/8361/7863EVM. Signals A0, M0, and M1 are configured with pull-up resistors by default. The jumper shunts supplied with the EVM can be used to set these signals to logic low. These signals can also be connected to control signals in the user's system.

**Table 3. J5: Header**

| Pin Number | Signal | Description |
|---|---|---|
| J5.1 | M0 | Selects two-channel or four-channel mode |
| J5.3 | M1 | Selects between serial outputs A and B |
| J5.5 | A0 | Operates in conjunction with M0. See device data sheet for details. |
| J5.7 | OUT B | B channel secondary output |
| J5.2 to J5.8 (even) | DGND | Digital ground connections |


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# 4 Power Supplies

The ADS7861 EVM board requires 5 $V_{DC}$ for both the analog and digital sections of the ADC. While filters are provided for all power-supply inputs, optimal performance of the EVM requires a clean, well-regulated power source. Positive 5-$V_{DC}$ power is applied to J3 and J4 (pin 1 referenced to pin 2). The ADS8361 and ADS7863 each require 5 $V_{DC}$ for the analog supply located on J3, and 2.7 V to 5.5 $V_{DC}$ for the digital supply located on J4.

An alternate power source can be applied via J6 located on the bottom side of the printed circuit board (PCB). If a variable digital supply voltage is desired, completely remove the shunt jumper from W3. Apply a 100-mA current limited dc voltage of not more than 5.5 V to J4.

**NOTE:** The shunt jumper at location W3 should be placed across pin 2 and pin 3 for proper operation of the ADS7861. This configuration is the factory default condition for all device versions of the ADS7861/8361/7863EVM.

## 4.1 Reference Voltage

The ADS7861/8361/7863 can be configured to use its internal reference or external reference source through jumper W1 (see schematic appended to this document for details). If an external reference is desired, the shunt jumper on W1 should cover pins 2 and 3. The external reference is supplied through header/socket J1 pin 20 (J1.20).

# 5 EVM Operation

Apply a current limited (150 mA max) 5-$V_{DC}$ source to J3 and J4 before connecting the analog input signals and digital control signals.

## 5.1 Analog Input

The analog input source can be applied directly to header/socket J1 (top or bottom side) or through optional amplifier and signal conditioning modules. The analog input level should not exceed 5 $V_{PP}$.The analog input range is from –VREF to VREF (0 V to 5 $V_{DC}$) centered at 2.5 V.

## 5.2 Digital Control

The digital control signals can be applied directly to header/socket J2 (top or bottom side). The ADS7861/8361/7863EVM can also be connected directly to a DSP interface board. Consult the respective device product folder for a complete list of DSP interface cards and optional analog interface modules.

## 5.3 Default Jumper and Header Settings

Jumper W2 is provided to allow separation of the convert start (CONVST) and read (RD) signals. The factory default condition for the EVM is to place a shunt jumper between pin 1 and pin 2 of W2. This configuration combines signals RD and CONVST, which are applied to the ADC via pin J2.7. When W2 is moved to pin 2 and pin 3, the RD signal is applied via pin J2.7 while CONVST is applied to pin J2.17.

Header J5 provides a way to access the M0, M1, and A1 control lines as well as the OUTB serial data. Shunt jumpers are placed on pins 1 and 2, 3 and 4, and 5 and 6 of J5, which defaults M0, M1, and A0 to logic low levels. Removing the jumpers allows these lines to go to logic high levels through the associated pull-up resistors R12, R13, and R14. In the factory default configuration, the ADC converts the A0 and B0 inputs, and places AOUT serial data on pin J2.13, and BOUT serial data on pin J5.7.


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# 6 Schematic, Bill of Materials, and Layout

A schematic for the ADS7861/8361/7863EVM is appended to this user's guide. The bill of materials is provided in Table 4.

## 6.1 Bill of Materials

**NOTE:** All components should be compliant with the European Union Restriction on Use of Hazardous Substances (RoHS) Directive. Some part numbers may be either leaded or RoHS. Verify that purchased components are RoHS-compliant. (For more information about TI's position on RoHS compliance, see the Quality and Eco-Info information on the TI web site.)

**Table 4. Bill of Materials**

| Item No. | Qty | | | Ref Des | Description | Vendor | Part Number |
|---|---|---|---|---|---|---|---|
| | ADS7861 | ADS8361 | ADS7863 | | | | |
| 1 | 1 | 1 | 1 | N/A | Printed Wiring Board | – | – |
| 2 | 8 | 8 | 8 | C1 to C8 | 100pF, 0603, Ceramic, C0G, 50V, 5% | Murata | GRM1885C1H101JA01D |
| 3 | 5 | 5 | 5 | C9, C10, C11, C12, C22 | 1000pF, 0603, Ceramic, C0G, 50V, 5% | Murata | GRM1885C1H102JA01D |
| 4 | 5 | 5 | 5 | C13, C14, C15, C16, C23 | 0.1µF, 0603, Ceramic, X7R, 50V, 10% | Murata | GRM188R71H103KA01D |
| 5 | 2 | 2 | 2 | C17, C18 | 10µF, 0805, Ceramic, X5R, 10V, 10% | Murata | GRM219R61A106KE44D |
| 6 | 2 | 2 | 2 | C19, C20 | 1.0µF, 0603, Ceramic, X5R, 16V, 10% | Murata | GRM185R61C105KE44D |
| 7 | 1 | 1 | 1 | C21 | 0.47µF, 0603, Ceramic, X7R, 16V, 10% | Murata | GRM188R71C474KA88D |
| 8 | 2 | 2 | 2 | L1, L2 | Ferrite Chip 600Ω 500MA 0805 | TDK | MMZ2012R601A |
| 9 | 2 | 2 | 2 | J1, J2 (top side) | 10-Pin, Dual Row, SMT Header (20 Pos.) | Samtec | TSM-110-01-T-DV-P |
| 10 | 2 | 2 | 2 | J1B, J2B (bottom side) | 10-Pin, Dual Row, SMT Socket (20 Pos.) | Samtec | SSW-110-22-F-D-VS-K |
| 11 | 2 | 2 | 2 | J3, J4 | 2 Terminal Screw Connector | OST | ED555/2DS |
| 12 | 1 | 1 | 1 | J5 | 4-Pin, Dual Row, TH Header (8 Pos.) | Samtec | TSW-104-07-L-D |
| 13 | 1 | 1 | 1 | J6 (bottom side) | 5-Pin, Dual Row, SMT Socket (10 Pos.) | Samtec | SSW-105-22-F-D-VS-K |
| 14 | 0 | 0 | 0 | W1 | Not installed | | |
| 15 | 2 | 2 | 2 | W2, W3 | 3-Pin header | Samtec | TSW-103-07-L-S |
| 16 | 2 | 2 | 2 | W4, W5 | 3-Pin , 2mm header | Samtec | TMM-103-01-T-S |
| 17 | 10 | 10 | 10 | R1 to R8, R14, R15 | 49.9Ω, 0603, 1%, 1/10W | Yageo | RC0603FR-0749R9L |
| 18 | 2 | 2 | 2 | R9 R10 | 33Ω, 0603, 1%, 1/10W | Yageo | RC0603FR-0733RL |
| 19 | 3 | 3 | 3 | R11 R12 R13 | 10Ω, 0603, 1% 1/10W | Yageo | RC0603FR-0710KL |
| 20 | 0 | 0 | 0 | R16 | Not installed | – | – |
| 21 | 1 | 1 | 1 | TP1 | Red Test Point Loop | Keystone | 5000 |
| 22 | 2 | 2 | 2 | TP2 TP3 | Black Test Point Loop | Keystone | 5001 |
| 23 | 1 | 0 | 0 | U1 | IC, ADC Dual 16-Bit 500kSPS 24QSOP | TI | ADS7861E |
| | 0 | 1 | 0 | | IC, ADC Dual 16-Bit 500kSPS 24QSOP | TI | ADS8361IDBQ |
| | 0 | 0 | 1 | | IC, ADC 12-Bit SER 2M 24QSOP | TI | ADS7863IDBQ |
| 24 | 1 | 1 | 1 | U2 | IC EEPROM 256kBIT 400KHz 8TSSOP | Microchip | 24AA256-I/ST |
| 25 | 1 | 1 | 1 | U3 | IC OPAMP GP R-R 50MHz DUAL 8SOIC | TI | OPA2365AID |


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# Revision History

| Changes from Original (October, 2002) to A Revision | Page |
|---|---|
| • Updated entire document to current standards | 1 |
| • Added ADS7863EVM to document contents | 1 |
| • Added figure of EVM | 1 |

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.


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| Revision History | | |
|---|---|---|
| REV | ECN Number | Approved |
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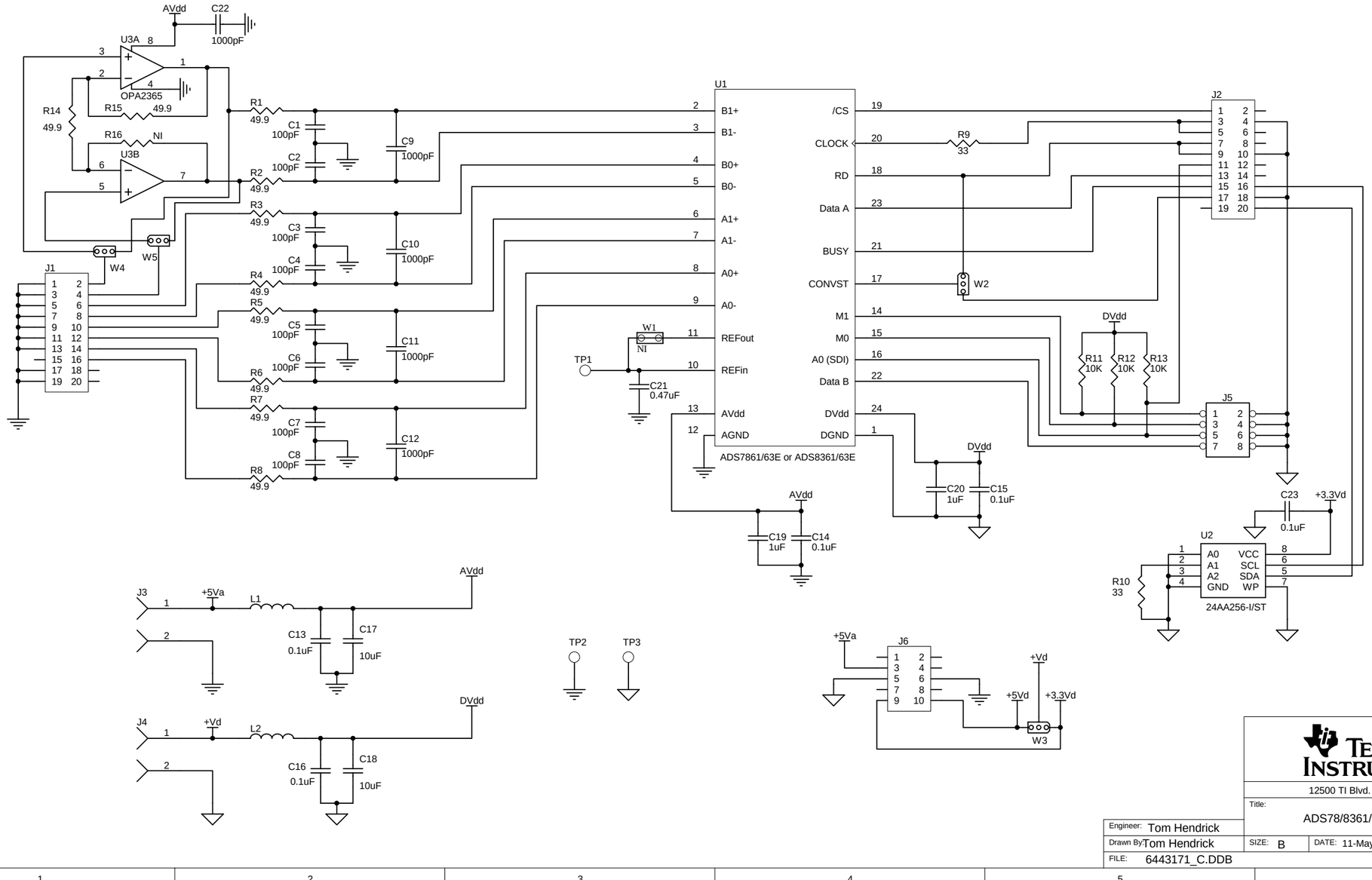



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|---|---|---|---|
| Title: ADS78/8361/7863 EVM Schematic | | | |
| Engineer: Tom Hendrick | | | |
| Drawn By: Tom Hendrick | SIZE: B | DATE: 11-May-2011 | REV: C |
| FILE: 6443171_C.DDB | | | SHEET: 1 OF: 1 |

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## EVM Warnings and Restrictions

It is important to operate this EVM within the input voltage range of 3.3 VDC to 5 VDC and the output voltage range of 0 VDC to 5 VDC.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

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