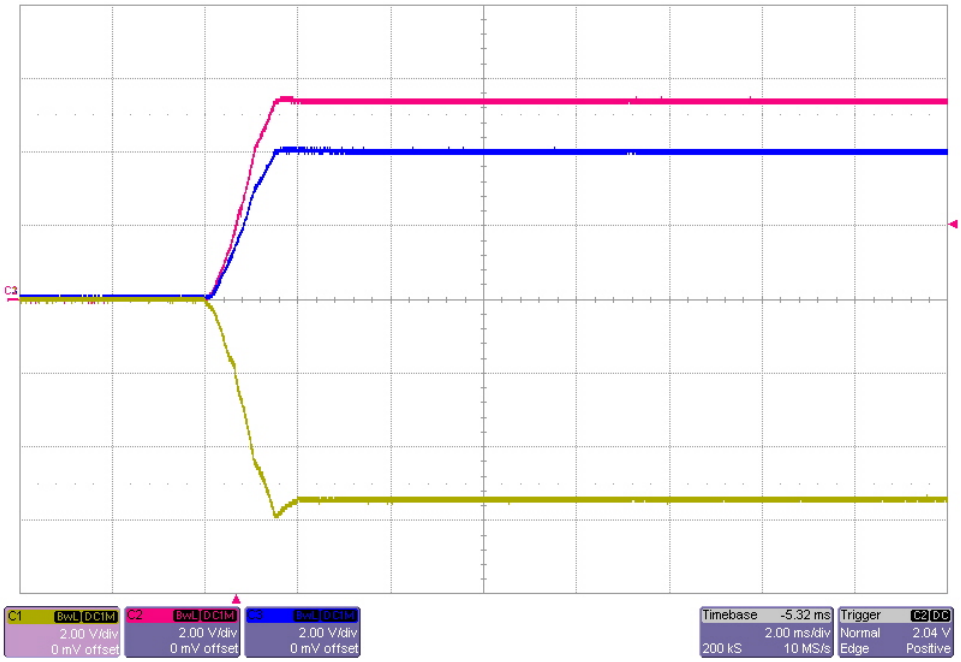
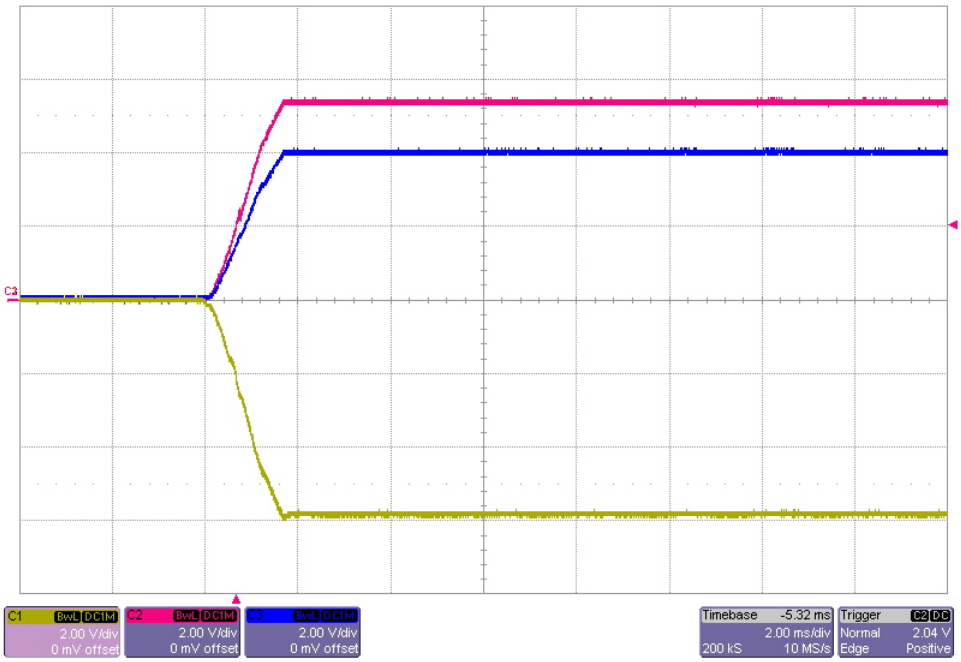
1 Startup

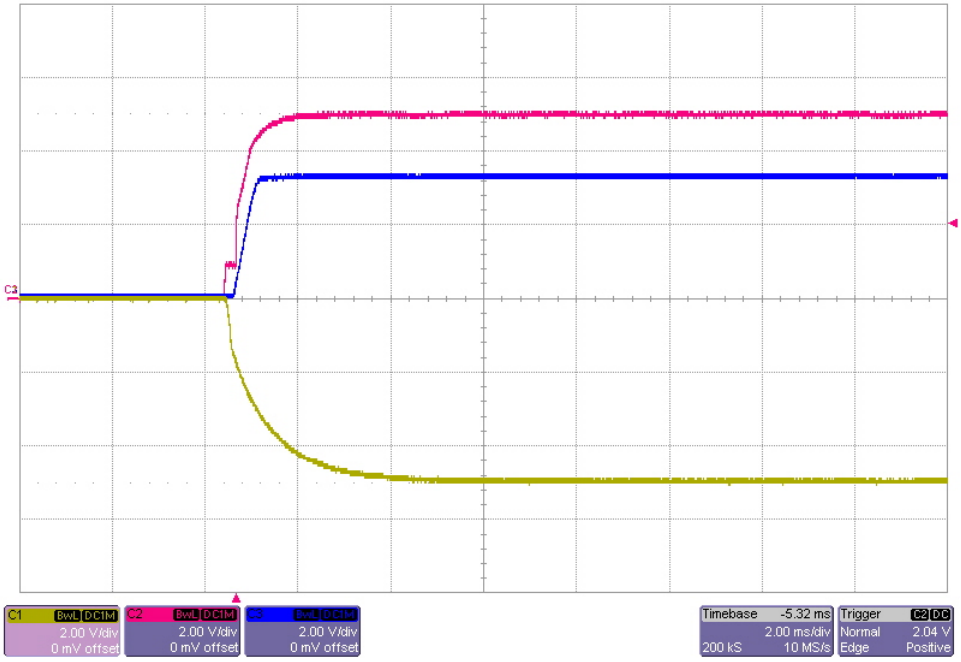
The photo below shows the flyback converter startup waveforms for the +4V, +5.5V and -5.75V output voltages after the application of 12Vdc in. The outputs were loaded to 0A. (2V/DIV, 2mS/DIV)



The photo below shows the flyback converter startup waveforms for the +4V, +5.5V and -5.75V output voltages after the application of 12Vdc in. The outputs were loaded to max loads. (2V/DIV, 2mS/DIV)

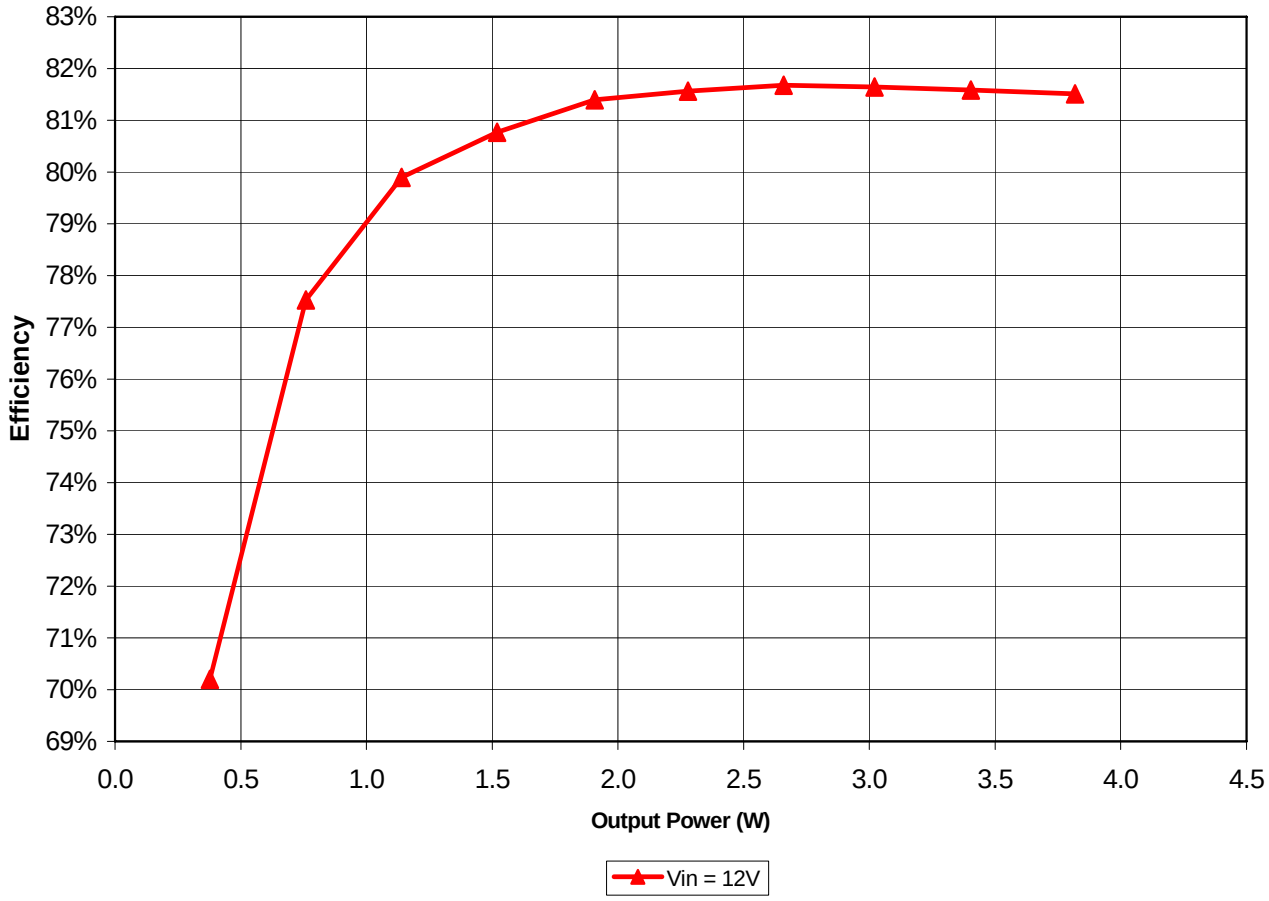


The photo below shows the linear regulator output voltage startup waveforms for the +3.3V, +5V and -5V output voltages after the application of 12Vdc in. The outputs were loaded to 0A. (2V/DIV, 2mS/DIV)



2 Efficiency

The flyback converter efficiency is shown in the figure below. The data does not include the losses in the linear regulators. Vin = 12V



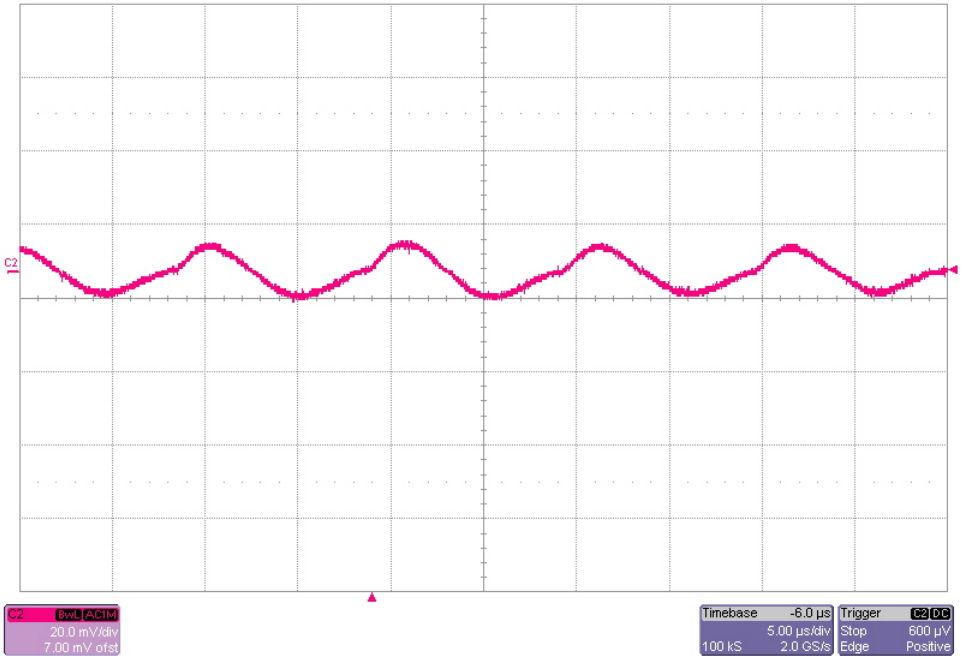
3 Cross Regulation

The table below shows the cross regulation between the three rectified transformer secondary voltages.
Vin = 12V

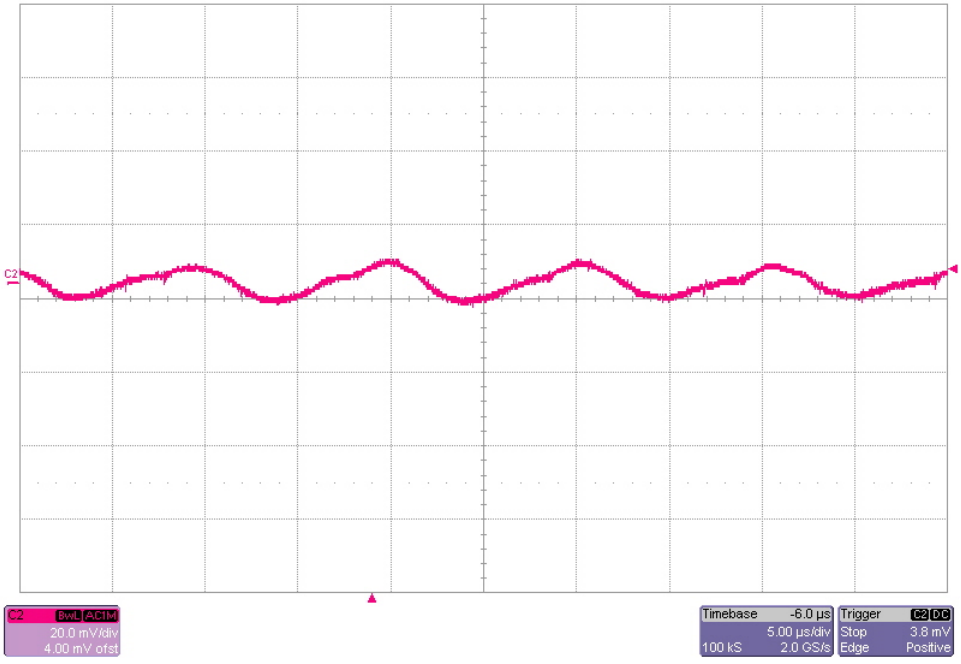
5.5V	4.0V	-5.75V
5.44V @ 0.5A	4.02V @ 0.25A	-5.839V @ 10mA
5.44V @ 0.5A	4.02V @ 0.25A	-7.59V @ 0A
5.44V @ 0.5A	4.36V @ 0A	-5.80V @ 10mA
5.44V @ 0.5A	4.42V @ 0A	-7.27V @ 0A
5.44V @ 0A	3.73V @ 0.25A	-5.374V @ 10mA
5.44V @ 0A	3.64V @ 0.25A	-6.161V @ 0A
5.44V @ 0A	4.01V @ 0A	-5.258V @ 10mA
5.44V @ 0A	4.00V @ 0A	-5.448V @ 0A

4 Output Ripple Voltage

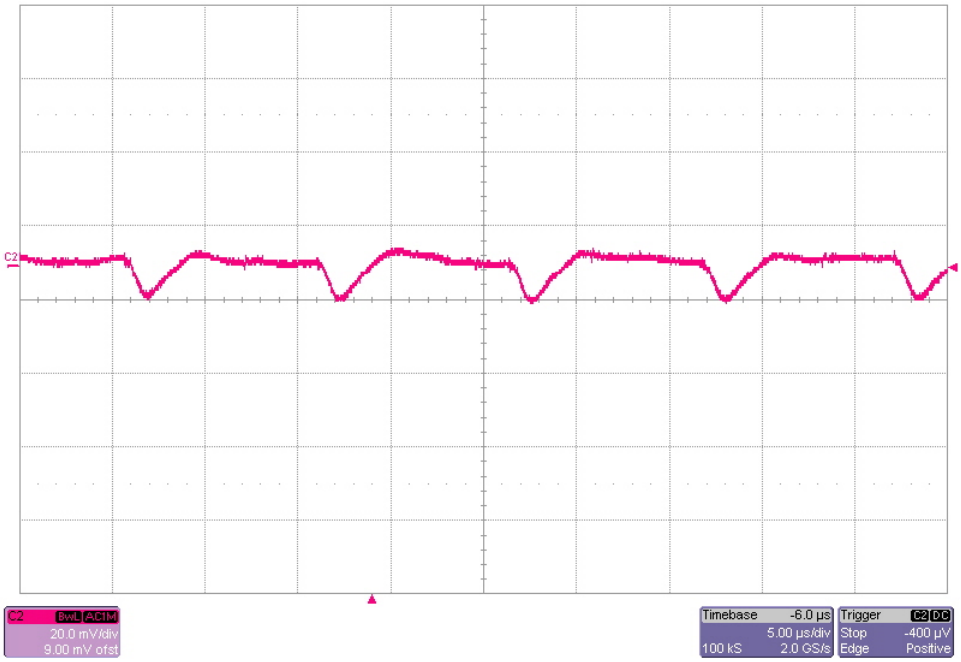
The +5V output ripple voltage is shown in the figure below. The image was taken with the 5V linear regulator loaded to 0.5A and the input voltage set to 12Vdc. (20mV/DIV, 5uS/DIV)



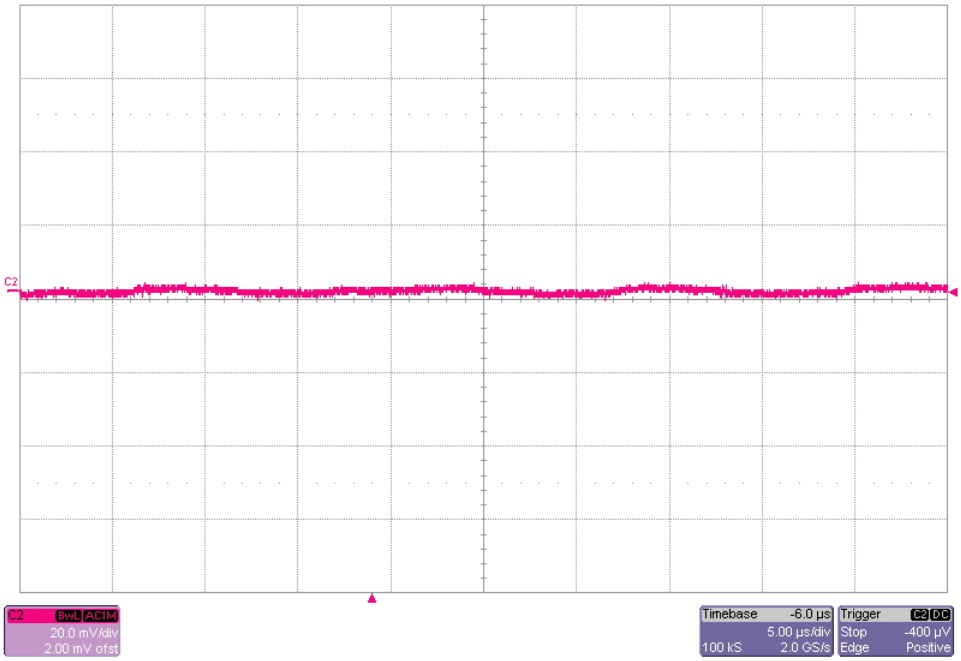
The 3.3V output ripple voltage is shown in the figure below. The image was taken with the 3.3V linear regulator loaded to 0.25A and the input voltage set to 12Vdc. (20mV/DIV, 5uS/DIV)



The -5V output ripple voltage is shown in the figure below. The image was taken with the -5V linear regulator loaded to 0.01A and the input voltage set to 12Vdc. (20mV/DIV, 5uS/DIV)

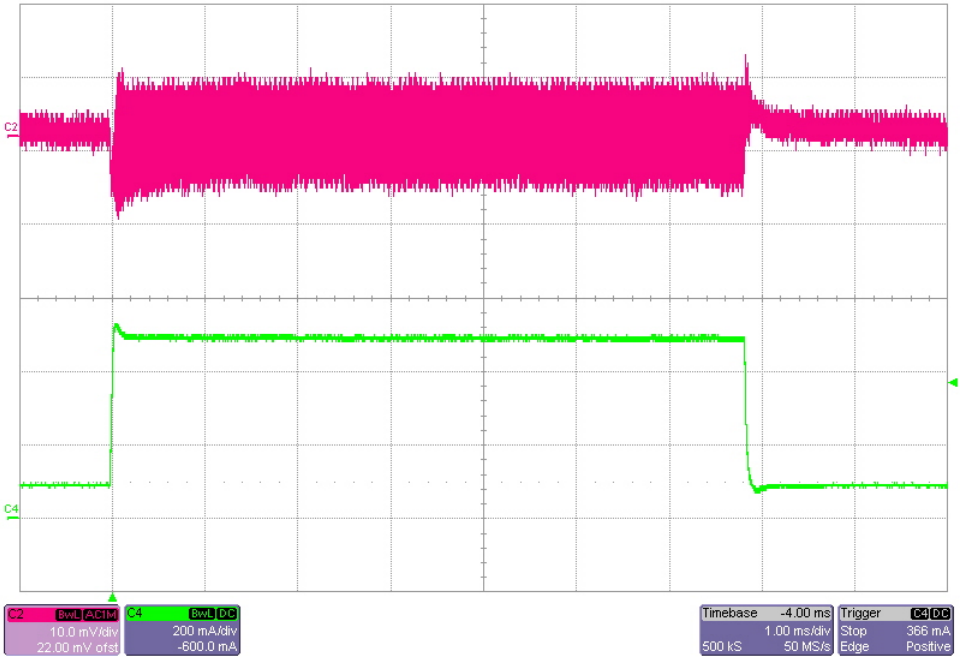


The 2.5V output ripple voltage is shown in the figure below. The image was taken with the 5V linear regulator loaded to 0.002A and the input voltage set to 12Vdc. (20mV/DIV, 5uS/DIV)

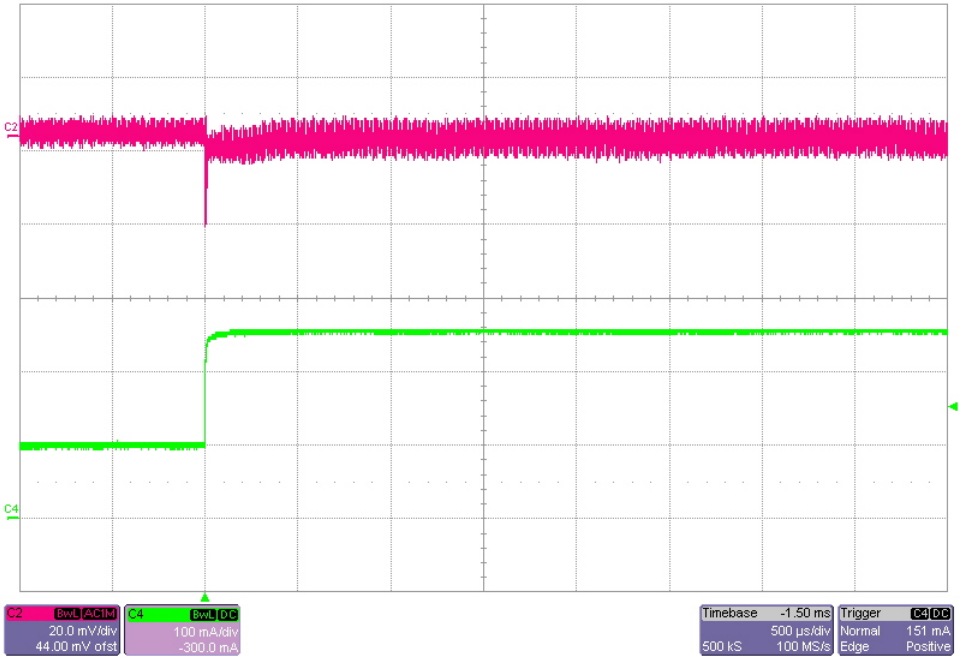


5 Load Transients

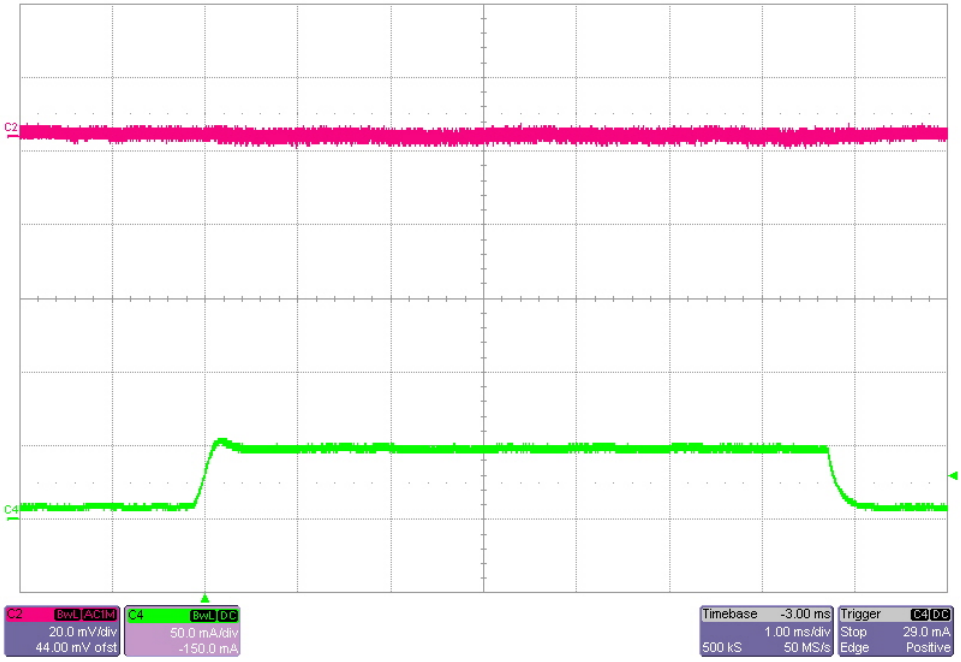
The photo below shows the 5V output voltage when the load current is stepped between 0.1A and 0.5A. Vin = 12Vdc. (10mV/DIV, 200mA/DIV, 1mS/DIV)



The photo below shows the 3.3V output voltage when the load current is stepped between 0.1A and 0.25A. Vin = 12Vdc. (20mV/DIV, 100mA/DIV, 500uS/DIV)

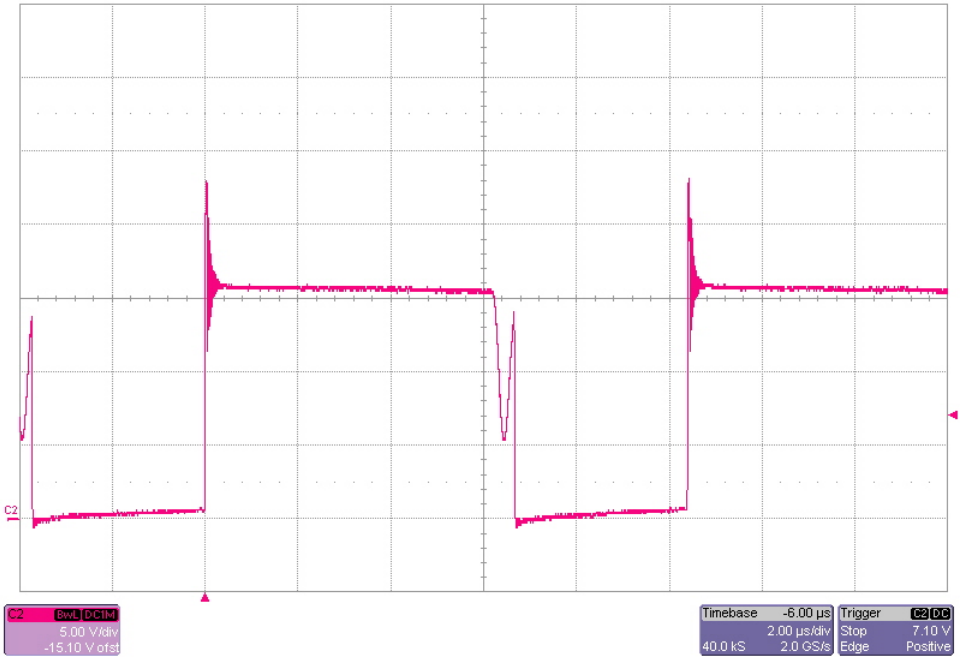


The photo below shows the (low current) 5V output voltage when the load current is stepped between 0.01A and 0.05A. Vin = 12Vdc. (20mV/DIV, 50mA/DIV, 1mS/DIV)

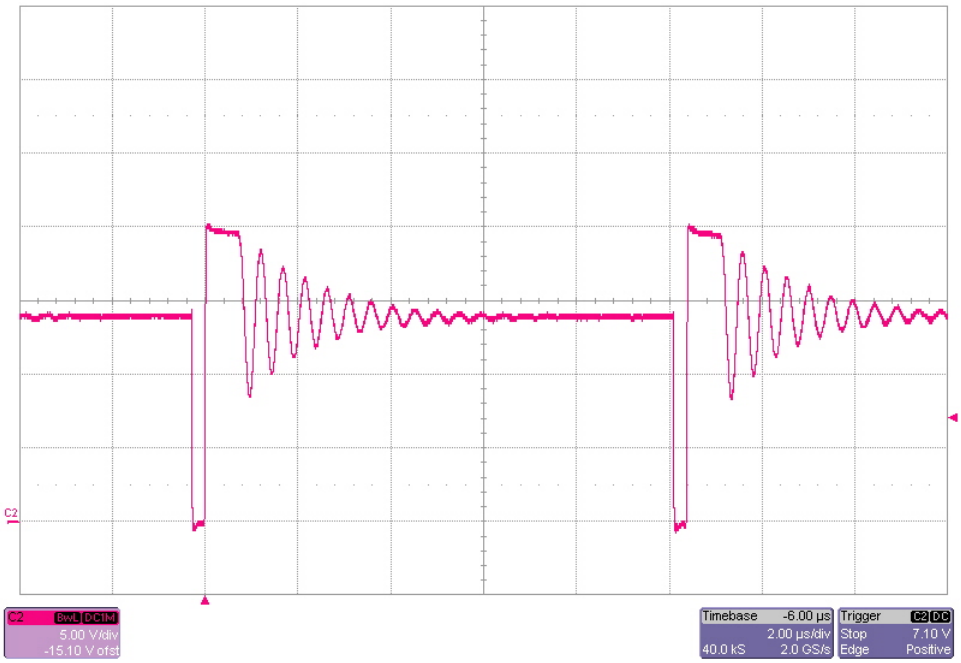


6 Switch Node Waveforms

The photo below is of FET Q1 switch node (TP11). The input voltage is 10Vand the outputs are loaded at max loads. (5V/DIV, 2uS/DIV)

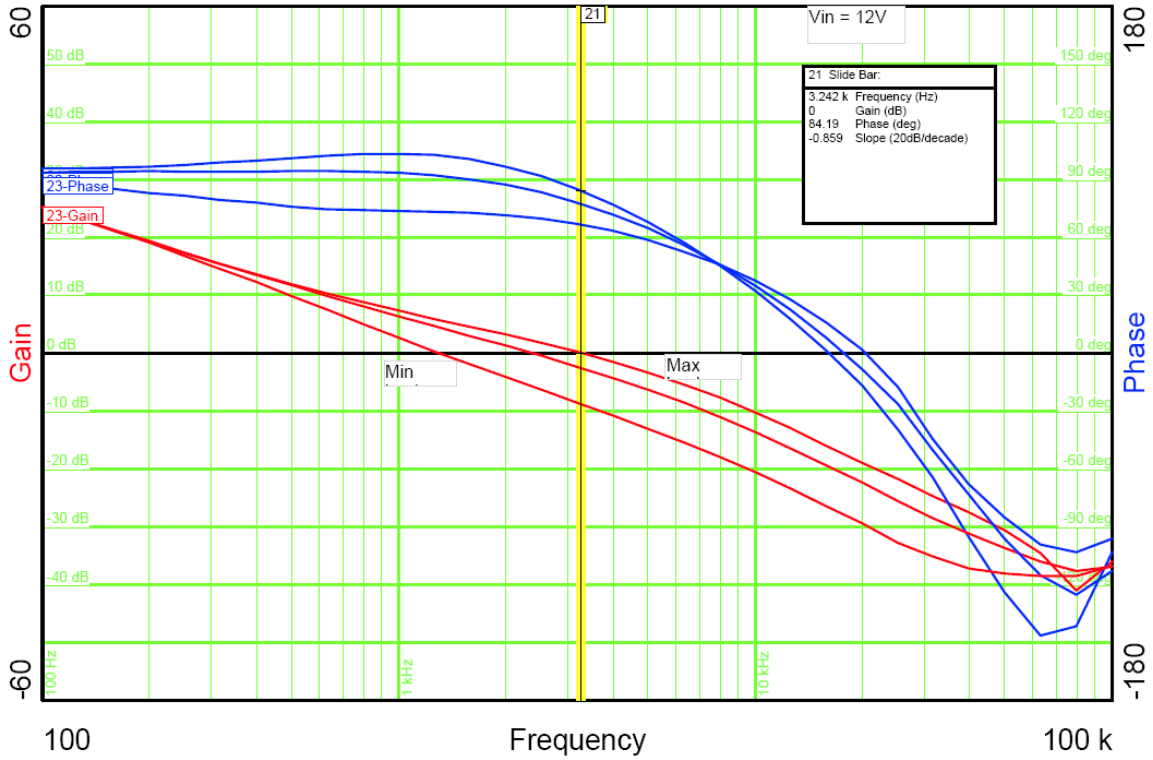


The photo below is of FET Q1 switch node (TP11). The input voltage is 14Vand the outputs are loaded at 0A. (5V/DIV, 2uS/DIV)



7 Control Loop Gain / Stability

The plot below shows the control loop gain and phase margin with the input voltage set to 12V. The outputs were loaded at min load (10% max), nominal (50% max) and max loads.



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